REMARKS

Claims 1-24 remain in the application for consideration of the Examiner with Clams 25 and 26 standing cancelled.

Reconsideration and withdrawal of the outstanding rejections are respectfully requested in light of the above amendments and following remarks.

Claims 1, 5, 6, 8, 12 , 13, 23, and 24 were rejected under 35 U.S.C. § 102(b) as being anticipated by Criscione; Claims 15, 18-20, 25, and 26 were rejected under 35 U.S.C. § 102(b) as being anticipated by Ellis; and Claims 15, 18-20, 25, and 26 were rejected under 35 U.S.C. § 102(b) as being anticipated by Matthews.

These rejections are respectfully traversed.

It is respectfully submitted that Criscione does not disclose or suggest the presently claimed invention including the cross coupled logic circuits as defined in independent Claims 1 and 8.

Additionally, Criscione does not disclose or suggest the presently claimed invention including the first logic level at the second output and the second logic level at the first output, the second logic level being opposite to the first logic level the first and second logic levels being non-overlapping to block cross conduction of current between the first and second voltage sources through the control circuitry as defined in independent Claim 23, additionally, Criscione does not disclose or suggest the first and second logic levels being non-overlapping to block cross conduction of current between the first and second voltage sources through the control circuitry in independent Claim 24.

The Examiner alleges that Criscione discloses cross couple logic circuitry in M8/M9 and M6/M3.

These are mere FET elements and not logic circuitry.

Ellis does not disclose or suggest the presently claimed invention including the hysteresis having negative temperature coefficients as defined in independent Claims 15 and 19.

The Examiner alleges that Figure 6 shows a comparator with hysteresis 22.

However, there is no indication that this hysteresis has a negative temperature coefficient as required by the claims in issue.

Likewise, Matthews does not disclose or suggest the presently claimed invention including the hysteresis having negative temperature coefficients as defined in independent Claims 15 and 19.

The Examiner alleges a comparator with hysteresis however again there is nothing to indicate a negative temperature coefficient.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

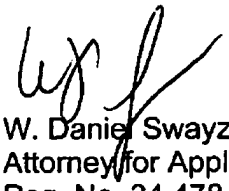
Applicants appreciate the indication that if Claims 2-4, 7, 9-11, 14, 16, and 17 were rewritten to include all the limitations of the base claim and any intervening claims, these claims would be allowable.

By the instant amendment, Claims 2, 7, 9, 14, and 16 have been placed in independent form.

Additionally, Applicants appreciate the indication that Claims 21 and 22 are allowed.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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